WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an insulator;

a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device;

a source region formed at a first end of the semiconductor layer, a height of the source region being higher than that of the fin;

a drain region formed at a second end of the semiconductor layer, a height of the drain region being higher than that of the fin; and

a metal gate region formed over to overlap at a top surface and at least one side surface of the fin.

2. The device of claim 1, wherein the metal gate region overlaps the top surface and two side surfaces of the fin.

3. The device of claim 1, further comprising:

oxide sidewalls formed adjacent the metal gate region in an area adjacent the top surface of the fin.

4. The device of claim 1, wherein the source and drain regions are silicided.

5. The device of claim 1, wherein a distance between the insulator and the metal gate region is about 500 Å to about 700 Å and a distance between the insulator and a top of the source or the drain region is about 600 Å to about 1000 Å.

6. The device of claim 1, wherein the metal gate comprises at least one of tungsten, titanium, nickel, TaSiN, and TaN.

7. A method for forming a semiconductor device comprising:

forming a semiconductor layer on an insulator;

forming a dummy gate structure over at least a portion of the semiconductor layer and a portion of the insulator;

etching the semiconductor device to remove the dummy gate structure and to create an area previously occupied by the dummy gate structure;

additionally etching the semiconductor device to decrease a width and height of the semiconductor layer in an area corresponding to a fin structure of the semiconductor device; and

depositing a metal layer in the area previously occupied by the dummy gate structure, the metal layer forming a gate for the semiconductor device.

8. The method of claim 7, wherein ends of the semiconductor layer on opposite sides of the metal layer form a source and drain region of the semiconductor device.

9. The method of claim 8, wherein a thickness of the fin structure ranges from about 500 Å to about 700 Å and a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å.

10. The method of claim 7, further comprising:

forming sidewall spacers adjacent the dummy gate structure in an area above the fin structure.

11. The method of claim 7, further comprising:

forming a protective layer over the semiconductor device after forming the dummy gate structure.

12. The method of claim 11, further comprising:

planarizing the protective layer to expose an upper surface of the dummy gate structure.

13. The method of claim 7, wherein the semiconductor device is a FinFET.

14. The method of claim 7, wherein the dummy gate structure is formed from polysilicon.

15. A FinFET device comprising:

an insulator;

a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device;

a source region formed from a first end of the semiconductor layer, a height of the source region being higher than that of the fin and a width of the source region being wider than that of the fin;

a drain region formed from a second end of the semiconductor layer, a height of the drain region being higher than that of the fin and a width of the drain region being wider than that of the fin;

a metal gate region formed to overlap at a top surface and at least one side surface of the fin; and

sidewalls spacers formed adjacent at least portions of the metal gate region.

16. The FinFET device of claim 15, wherein the sidewall spacers have a width ranging from about 150 Å to about 1000 Å.

17. The FinFET of claim 16, wherein the source and drain regions are silicided.

18. The FinFET of claim 1, wherein a thickness of the fin portion ranges from about 500 Å to about 700 Å and a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å.